XRD98L63EVAL

Evaluation System (Socketed) User Manual

1.0 EVALUATION SYSTEM PARTS LIST

- ·XRD98L63EVAL Application Printed Circuit Board
- ·XRD98L63 CCD Image Digitizer
- ·XRD98L63EVAL User Manual
- ·XRD98L63 Data Sheet

2.0 FEATURES

- ·Easy Evaluation of the XRD98L63 CDS, PGA, and ADC functions
- ·CCD Emulator on the PCB
- ·Analog & Digital Support Circuitry
- ·3V Evaluation
- ·Optimized and proven Layout
-

3.0 INTRODUCTION

The XRD98L63EVAL is a complete printed circuit test board designed to permit quick and accurate evaluation of EXAR's XRD98L63 Image Digitizer. The direct solder down of the XRD98L63 to the PCB allows for system and ADC noise evaluation without the impedances introduced by a socket. The XRD98L63 is an analog to digital interface for CCD video, digital, and pc cameras. The chip includes a correlated double sample & hold (CDS), a programmable gain amplifier (PGA), and a 12-bit analog to digital converter (ADC) with automatic offset calibration.

The XRD98L63EVAL is a four layer PCB with an optimized layout for 12-bit accurate conversions at greater than 30MHz sampling rates. The board contains the support circuitry for evaluation at 3V power supplies.

Pixel switching amplifiers (U3 & U4) emulate the output signal of a CCD by switching between two externally provided analog voltage sources. When the actual CCD is unavailable, this emulator provides a method to test the XRD98L63.

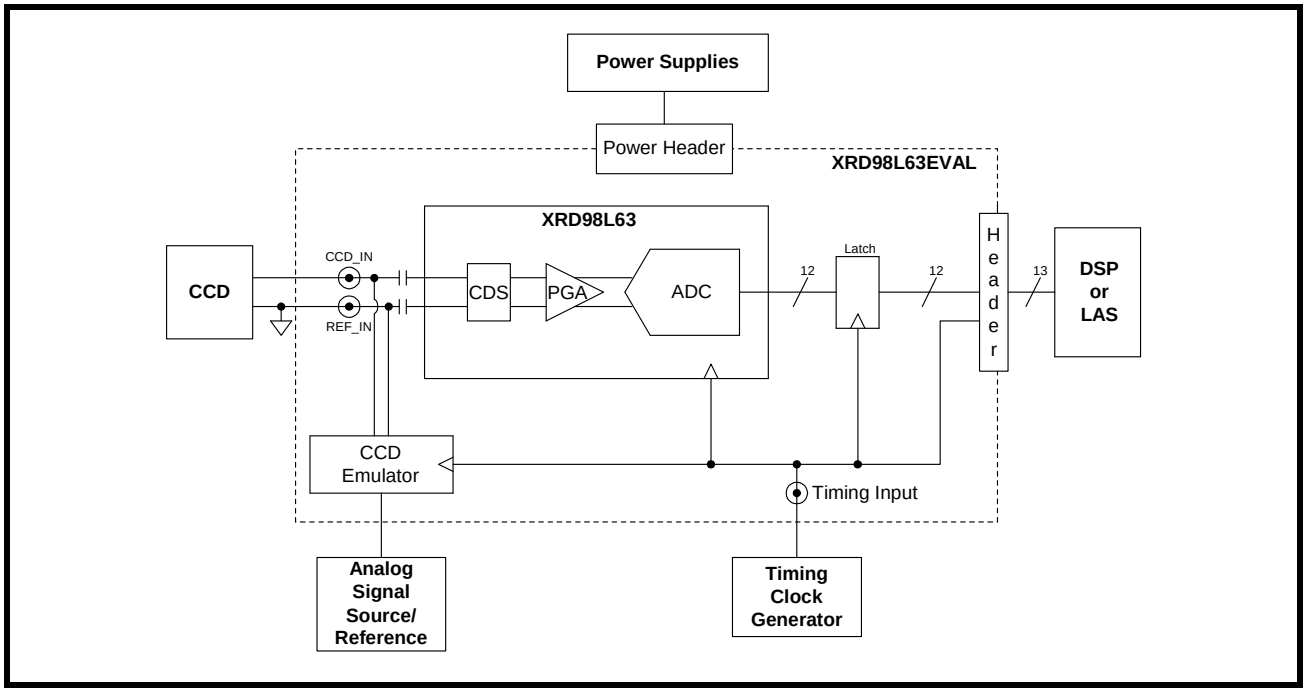


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM OF XRD98L63EVAL TEST SETUP

4.0 XRD9818EVAL APPLICATION CIRCUITRY

The XRD98L63EVAL is an evaluation PCB layout designed to test functionality and performance of the XRD98L63 The evaluation platform requires only power supplies, inputs to the CCD emulator and test equipment (Logic Analyzer, Oscilloscope) in order to evaluate most of the functional and performance aspects of the XRD98L63. The following sections describe the functional blocks that make up the XRD98L63EVAL system.

4.1 Timing Inputs

The XRD98L63 has multiple timing inputs that are needed for proper operation of the device. The timing required for the XRD98L63 can be broken into 4 distinct areas:

1. Pixel timing - timing used to correctly sample individual pixel data.
2. Line timing - timing used to perform the calibration and clamping functions against the CCD's optically black (OB) pixels.
3. Multi-Gain Mode Timing - timing used to define Frame and Line start for Multi-Gain operation.
4. Serial Port timing - 3-wire interface timing to write and read the internal registers of the XRD98L63.

4.1.1 Pixel Timing

The pixel timing inputs ADCLK, SBLK and SPIX all run at the pixel rate. ADCLK determines the internal sampling of the PGA output and data conversion of the ADC, SBLK defines the sampling point of the reference level of the CCD signal and SPIX defines the sampling point of video content for each pixel. The positioning of SBLK & SPIX with respect to the CCD signal and relationship of ADCLK, SBLK & SPIX to each other are detailed in the XRD98L63 data sheet

4.1.2 Line Timing

The line timing input signals are CAL, CLAMP & PBLK. The CAL input is used to define OB pixels from the CCD to be used for the auto-matic calibration out of offsets in the camera system. CLAMP is used to define the DC operation point of the input pins CCD_IN & REF_IN level shifting the CCD output to a usable range for the XRD98L63's inputs. PBLK is used to define the CCD vertical shift time period. Again, the proper placement and function of these three timing signals is defined in the XRD98L63 data sheet.

4.1.3 Multi-Gain Mode Timing

The multi-gain mode timing inputs are FSYNC and EOS. Many area array CCD's are commonly run in a continuous mode and are switched from a low res mode for view and a high res mode for capture. When operation in the Multi-Gain Mode the XRD98L63 must automatically adjust pixel gains according to the pattern of the particular CCD array. In order to do this the XRD98L63 must have an identifier for the start of a frame and start of each line. The FSYNC input is used to define start of frame for an area array CCD in a continuous output operation and the EOS input is used to define the start of each line. Please see the data sheet for a better description of this mode.

4.1.4 Serial Port Control

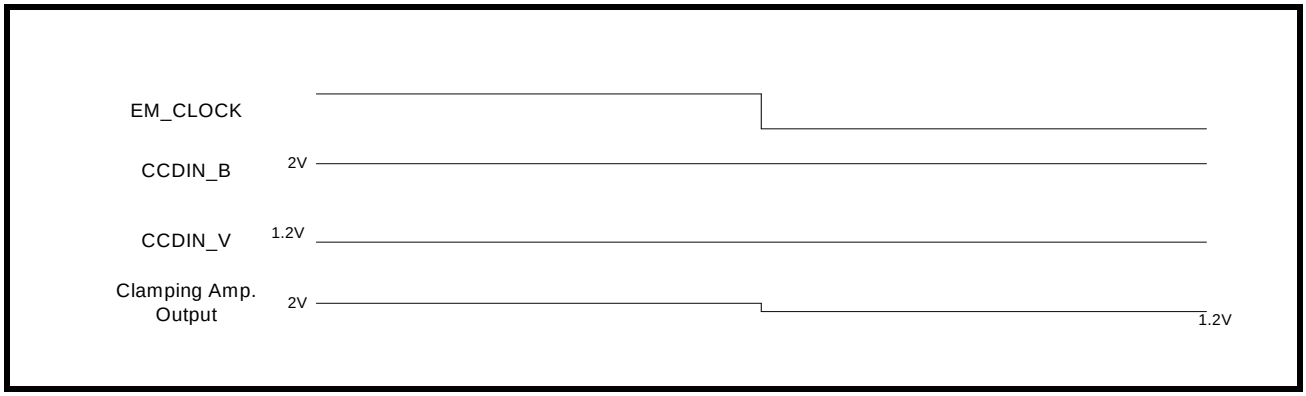
The Serial Port Control pins (LOAD, SDI & SCLK) are used to configure the XRD98L63. The timing requirements and register configuration are detailed in the XRD98L63 data sheet.

4.2 CCD Emulator Circuitry

The emulation circuitry is intended to provide a pseudo CCD signal in order to evaluate the XRD98L63 when configured for CCD operation. This is accomplished by the use of an clamping amplifier (AD8036) as seen in the evaluation board schematic. The basic function of the AD8036 (U3 & U4) is to switch between the its two inputs signals according to the polarity of the EM_CLOCK timing signal. The inputs for each channel will be used to emulate the black reference level and video level of a CCD signal. If you look at the Figure 2 below you will see that the EM_CLOCK connects the CCDIN_B (black reference level) input to the output when high

and the CCDIN_V (video level) when the EM_CLOCK is low. The resulting output signal as shown in the example timing for a CCDIN_B=2V and a CCDIN_V=1.2V is a 800mVpp signal toggling with the EM_CLOCK.

FIGURE 2. BASIC FUNCTION OF CLAMPING AMPLIFIER



To be able to test the XRD98L63 for DNL & INL (system linearity) specifications a sine wave generator can be connected to the Video input that has its peaks at 2V and 1.2V. This will cause the output of the XRD98L63 to generate a digital sinewave that goes can be scaled with the PGA gain code.

4.3 Digital Output Interface

The interface to a Logic Analyzer is provided by two 15x2 headers (S1 & S2). Each header provides 12 bits of data, latch clock and individual ground for each signal. S1 is an unbuffered direct connection to the 98L63's output pins while S2 is buffered. The latch clock input timing signal (LT CLK) is intended to identify that the data is valid and should be sampled by the logic analyzer.

5.0 XRD98L63EVAL SCHEMATICS

FIGURE 3. XRD98L63EVAL

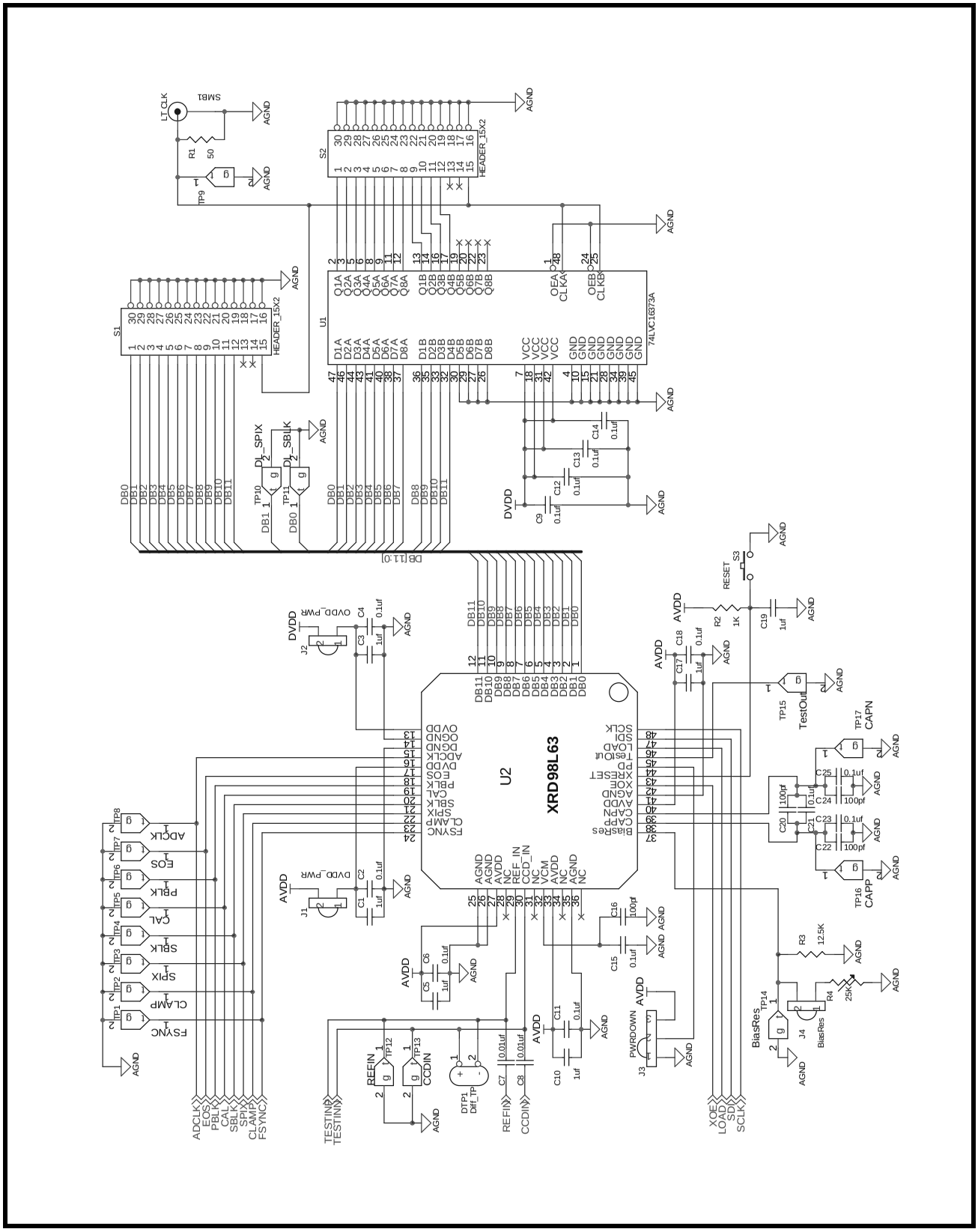


FIGURE 4. XRD98L63EVAL TESTIN INPUTS

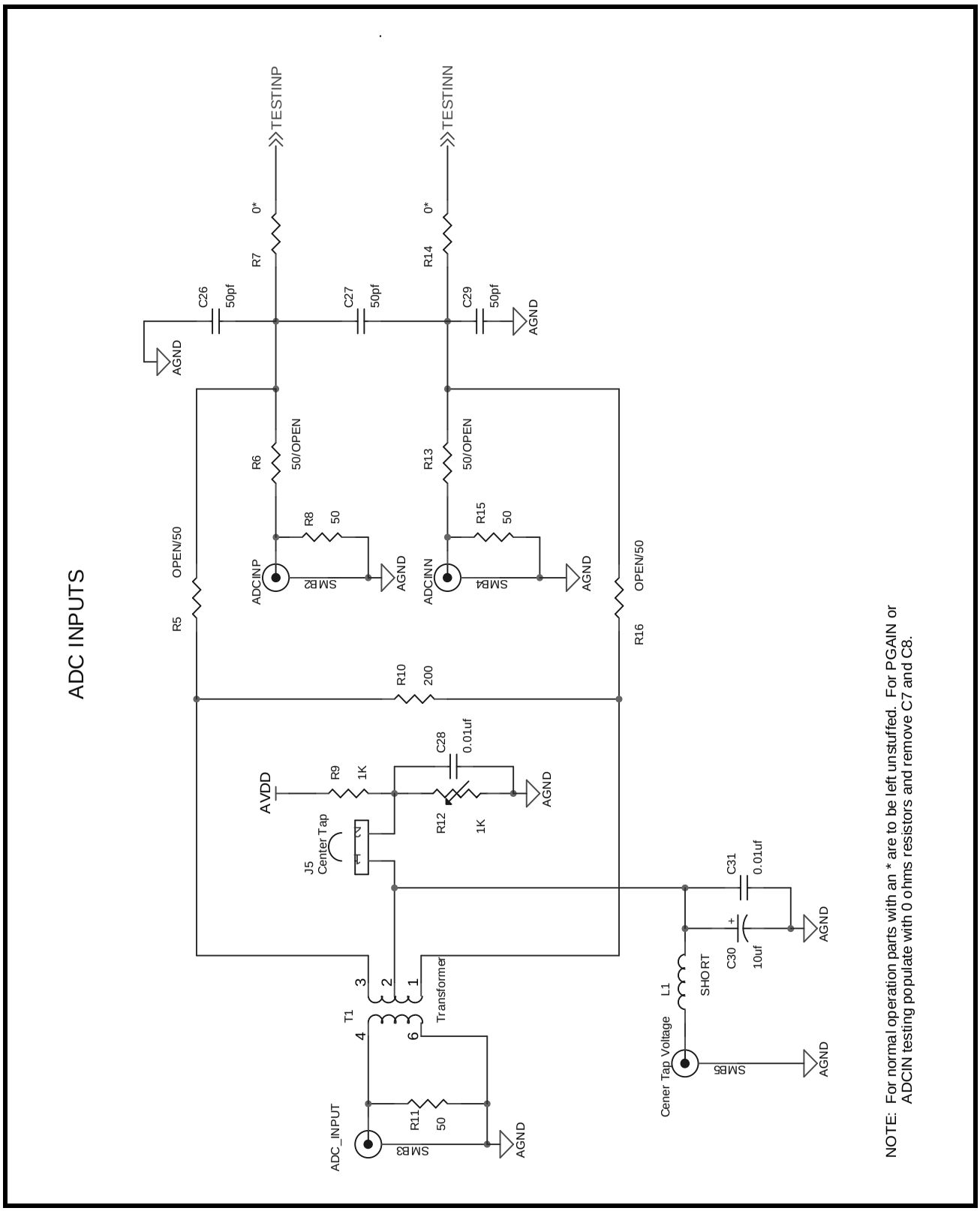


FIGURE 5. XRD98L63EVAL CCD EMULATOR

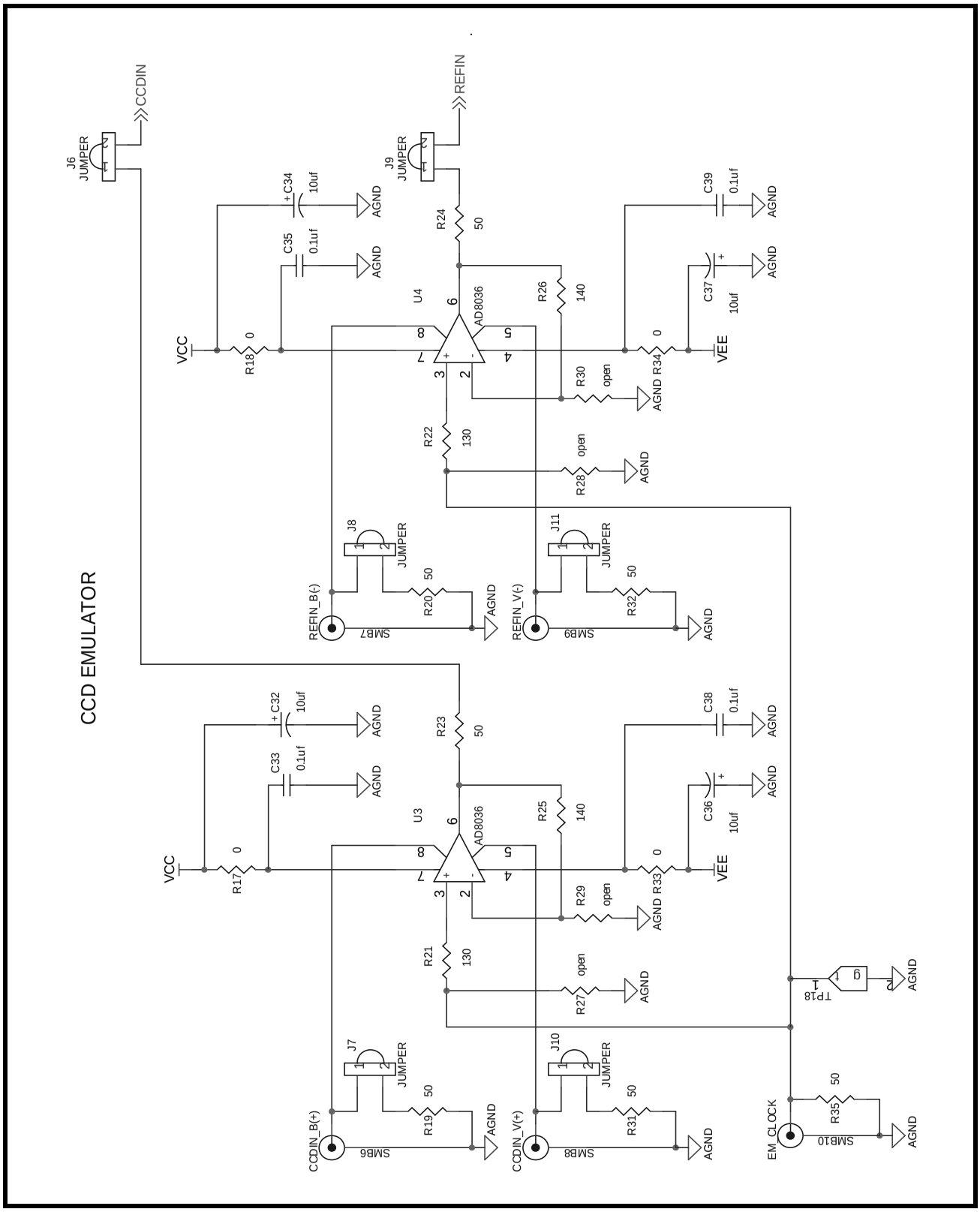


FIGURE 6. XRD98L63EVAL POWER HEADER

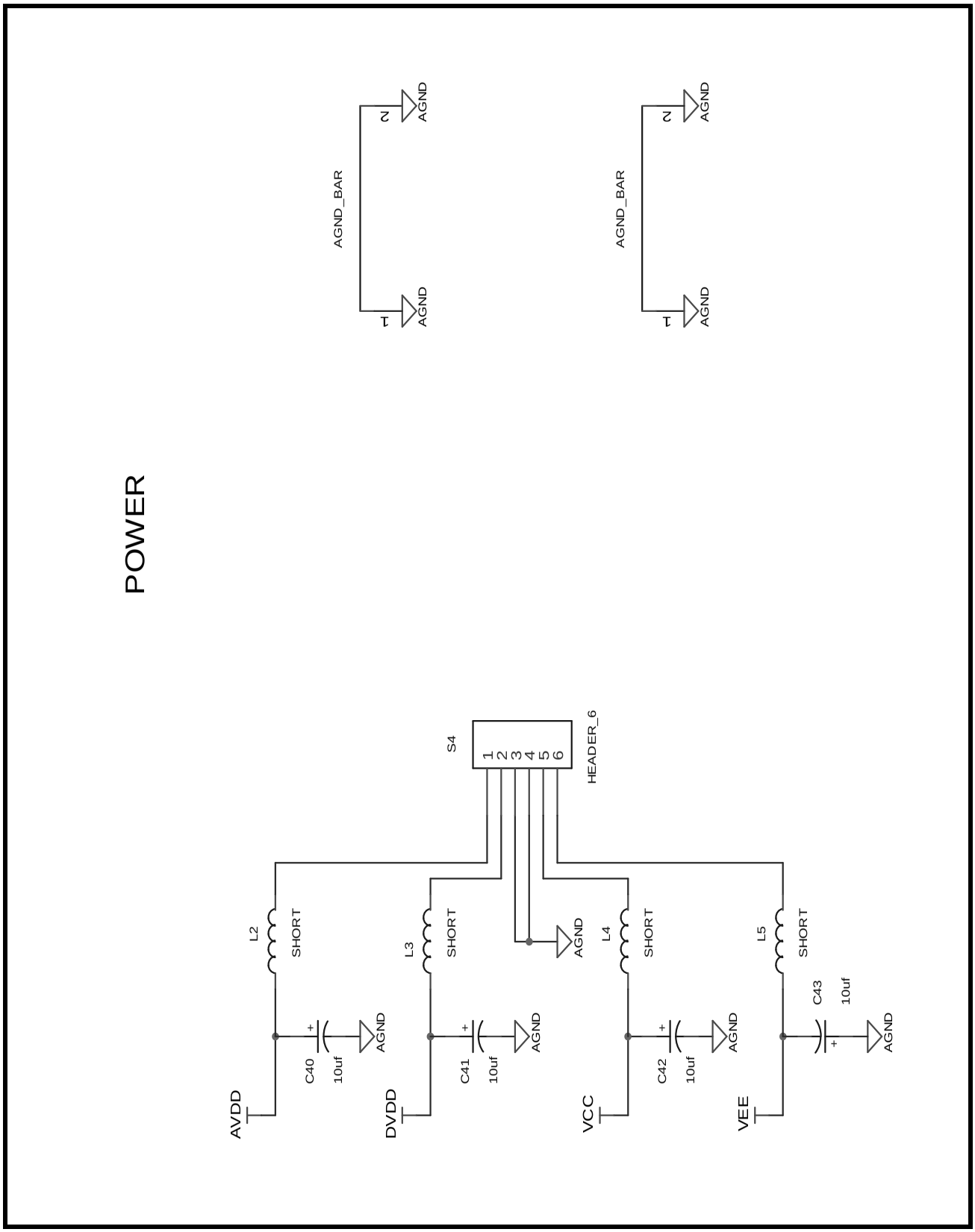


FIGURE 7. XRD98L63EVAL SMB CONNECTORS